IN THE CLAIMS

What is claimed is:

1. A system for processing simplex and multiplexed voice packets, comprising:

a compare circuit that includes a plurality of locations that include simplex entries and multiplex entries, each simplex entry including data that can match simplex packet information, each multiplex entry including data that can match multiplex packet information.

2. The system of claim 1, wherein:

each simplex entry includes data that can match predetermined simplex packet header information.

3. The system of claim 1, wherein:

each simplex entry includes data that can match information corresponding to at least one network layer.

4. The system of claim 1, wherein:

each simplex entry includes data that can match a user datagram protocol destination port address.

5. The system of claim 1, wherein:

each simplex and multiplex entry includes an entry type field having a

first value in a simplex entry and a second value different from the first value in a multiplex entry.

6. The system of claim 1, wherein:

the compare circuit includes a content addressable memory (CAM).

7. The system of claim 6, wherein:

the CAM includes maskable entries.

8. The system of claim 7, wherein:

the CAM entries are globally maskable.

9. A packet processing system, comprising:

a compare section having a content addressable memory (CAM) that includes a plurality of entries that match simplex voice packet information and multiplexed voice packet information.

10. The packet processing system of claim 9, wherein:

each entry includes at least one bit that indicates if the entry matches simplex voice packet information or multiplexed voice packet information.

11. The packet processing system of claim 9, wherein:

each entry that matches multiplexed voice packet information includes a field that stores a voice channel value.

12. The packet processing system of claim 11, wherein:

each entry that matches multiplexed voice packet information further includes a trunk field that stores a data value corresponding to a grouping of voice channels.

13. The packet processing system of claim 9, wherein:

each entry that matches simplex voice packet information includes a field that stores a voice channel value.

14. The packet processing system of claim 9, wherein:

each entry that matches simplex voice packet information includes a field that matches transport layer header information.

15. A system, comprising:

a processor;

a storage register coupled to the processor that stores simplex voice packet information;

a voice packet input coupled to the processor that provides multiplexed voice packet information; and

a compare circuit coupled to the processor that compares simplex voice packet information from the storage register and multiplexed voice packet information from the voice packet input to a plurality of entries, each entry indexing to a particular voice channel.

16. The system of claim 15, wherein:

the compare circuit includes a content addressable memory (CAM).

17. The system of claim 16, wherein:

each CAM entry includes at least one entry type field for distinguishing between entries that match simplex voice packet information and entries that match multiplexed voice packet information.

18. The system of claim 17, wherein:

each entry indexes address information for a storage location corresponding to a voice channel.

19. The system of claim 15, wherein:

the compare circuit entries each include valid indications that indicate when an entry contains valid information.

20. The system of claim 15, wherein:

the compare circuit compares simplex voice information with multiple entries.

21. The system of claim 15, wherein:

the compare circuit compares multiplex voice information with multiple entries.